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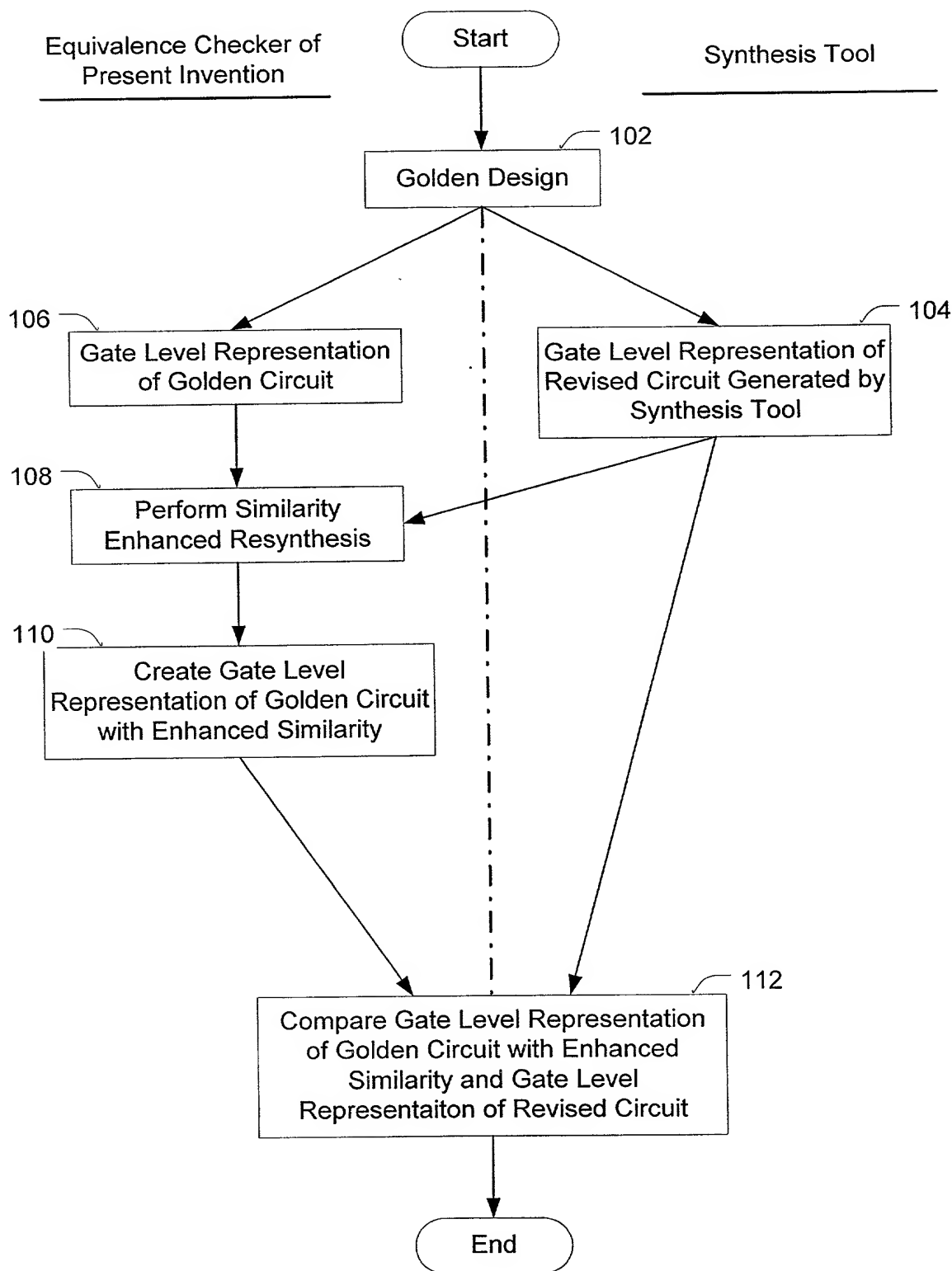


Fig. 1

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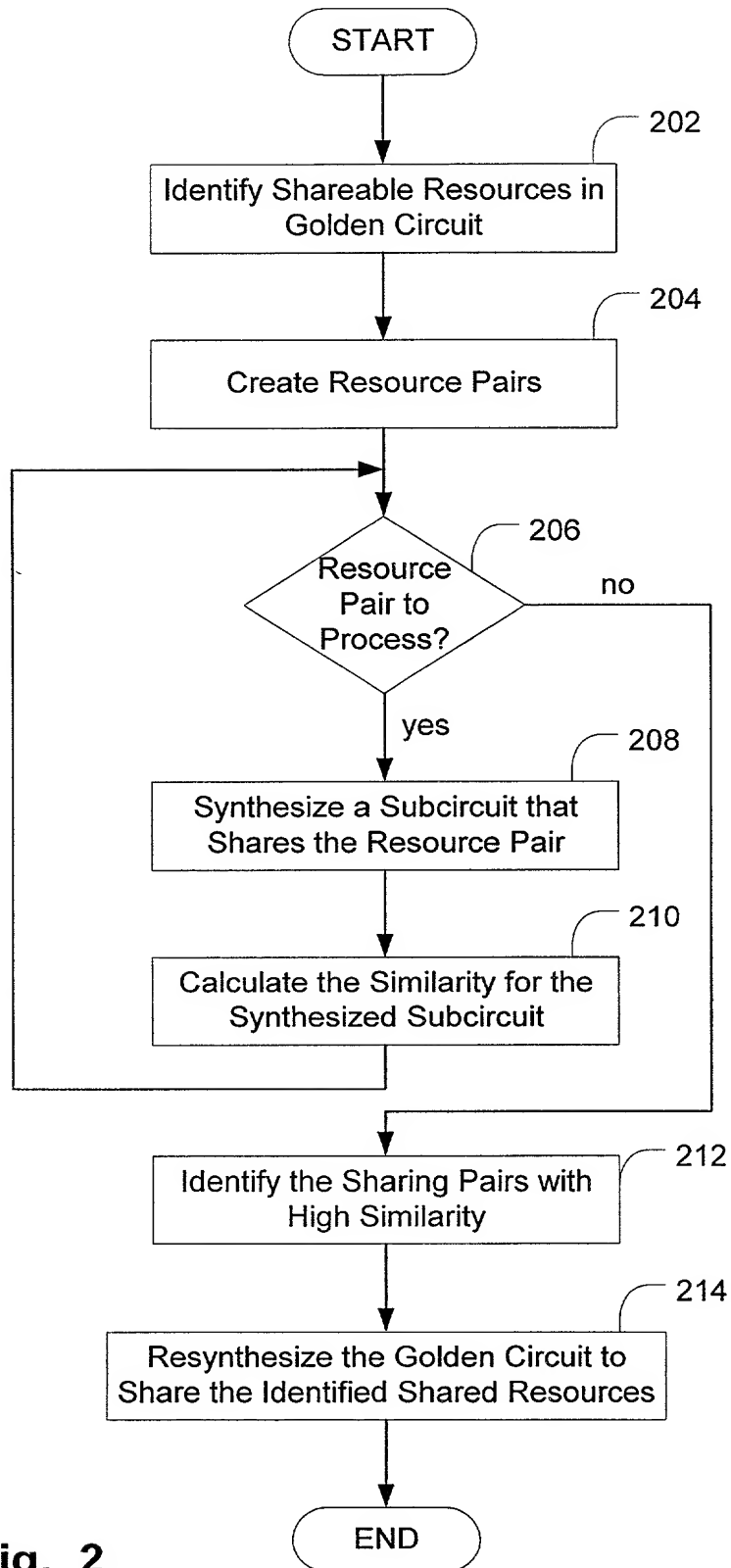


Fig. 2

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Verilog Example For Resource Sharing Learning

```
module example(in1,in2,in3,in4,in5,in6,in7,in8,sel,y);
input [3:0] in1,in2,in3,in4,in5,in6,in7,in8;
input [2:0] sel;
output [7:0] y;
reg [7:0] y;

always @(in1 or in2 or in3 or in4 or in5 or in6 or in7 or in8 or sel) begin
  case(sel)
    1:
      y = in1 * in2;    // multiplier m1
    2:
      y = in3 * in4;    // multiplier m2
    3:
      y = in5 * in6;    // multiplier m3
    default:
      y = in7 * in8;    // multiplier m4
  endcase
end

endmodule
```

Fig. 3

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(a) Sharing Pair Examples

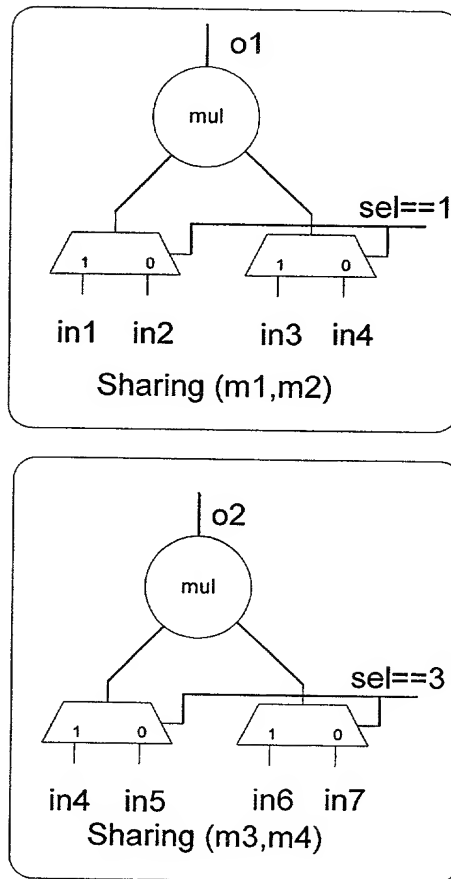


Fig. 4A

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(b) Golden Circuit

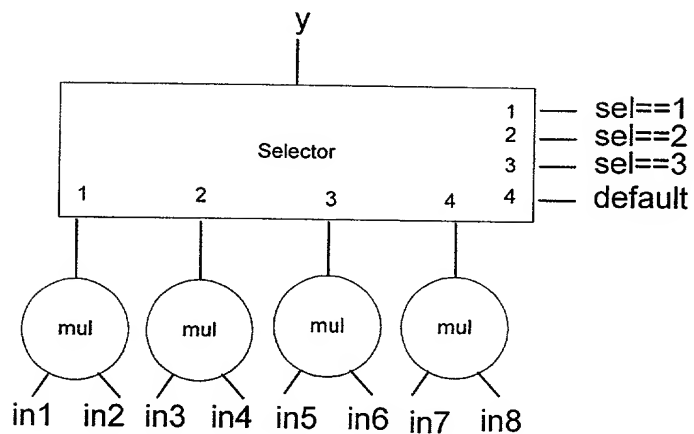


Fig. 4B

(c) Revised Circuit

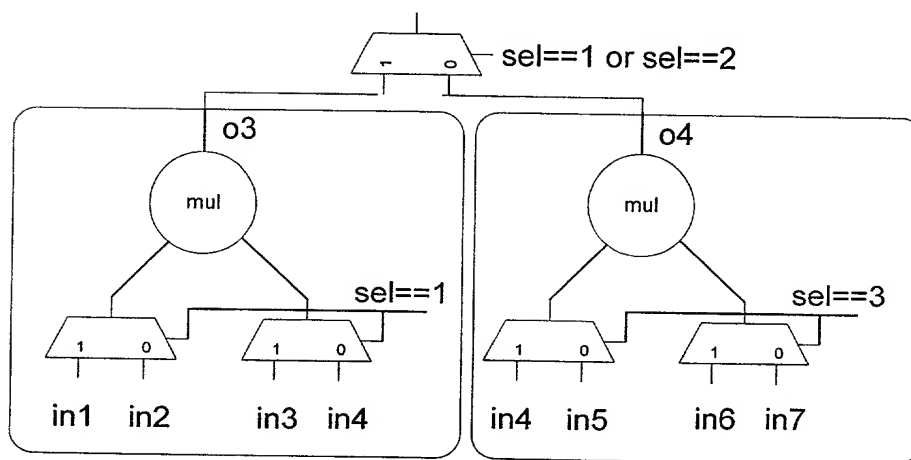


Fig. 4C

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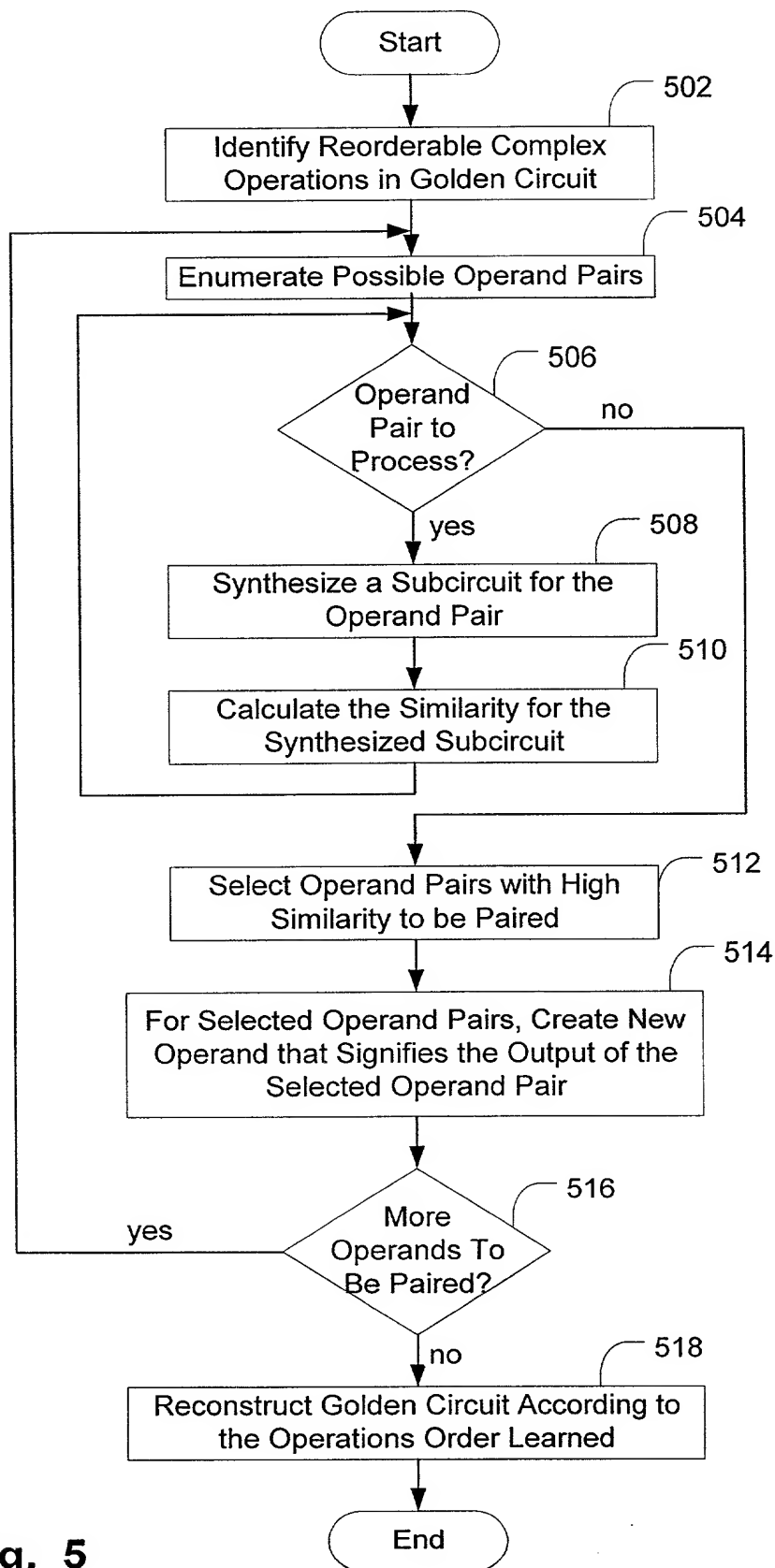


Fig. 5

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(a) Golden Netlist

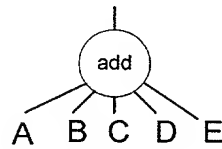


Fig. 6A

(b) Revised Netlist

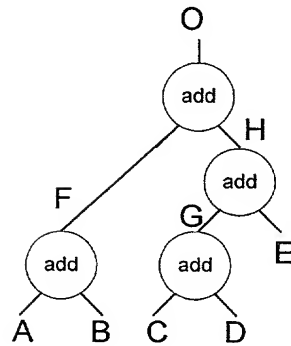


Fig. 6B

(c) Learning Steps

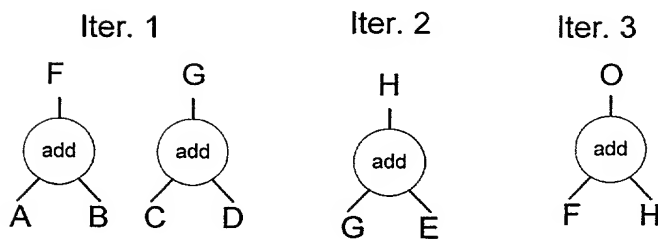


Fig. 6C

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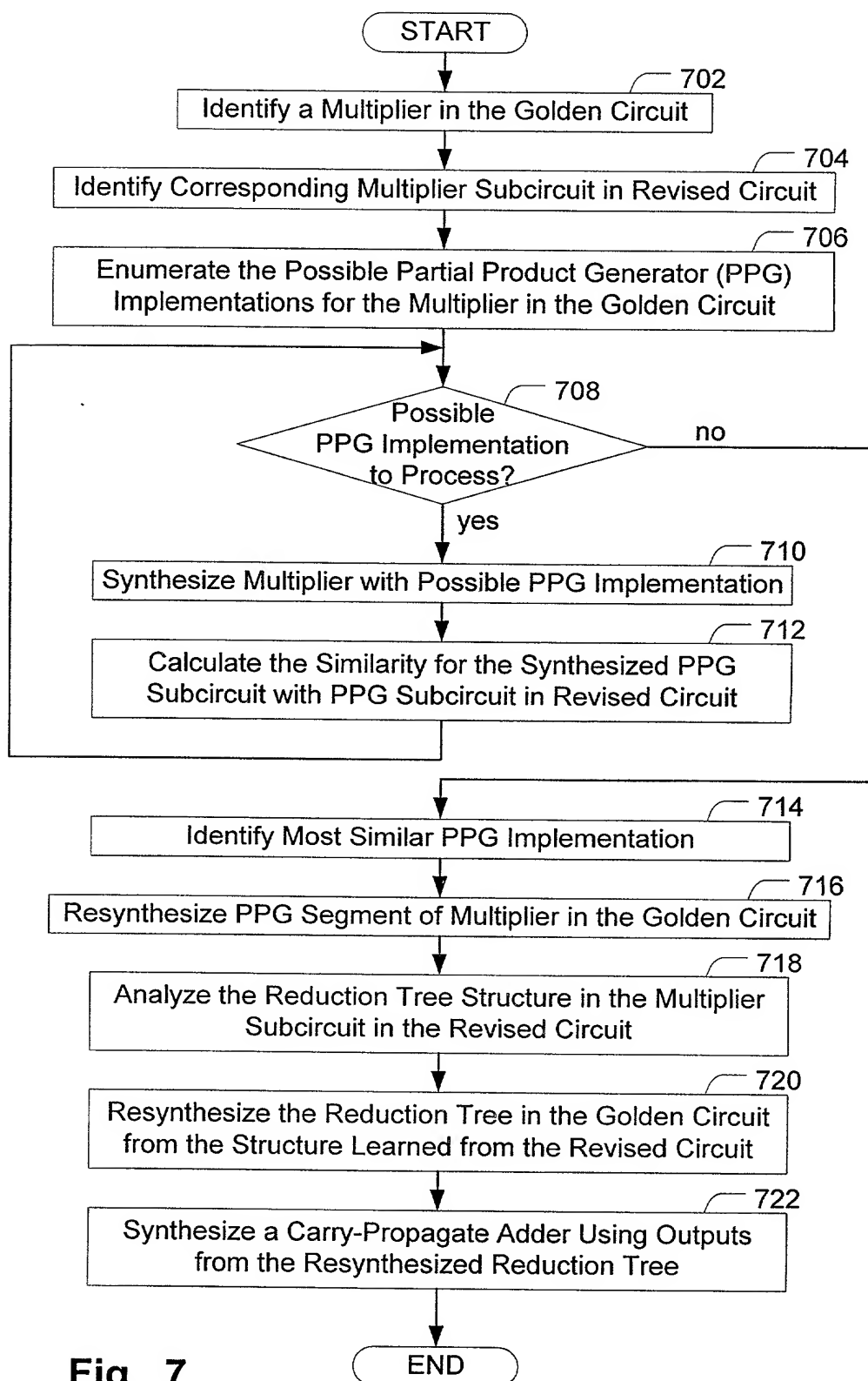


Fig. 7

Column	6	5	4	3	2	1	0
Weight	2^6	2^5	2^4	2^3	2^2	2^1	2^0

